CLAIMS

1. An insulated gate device comprising a gate connected to a gate terminal and having a variable input capacitance at the gate terminal as the device is switched between an off state and an on state, a ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller than 2.0.

2. A device as claimed in claim 1 comprising a power metal oxide silicon field effect transistor (MOSFET).

3. A device as claimed in claim I or claim 2 wherein the ratio is less than 1.5.

4. A device as claimed in claim 3 wherein the ratio is substantially equal to 1.

5. A device as claimed in any one of claims 1 to 4 comprising a capacitor connected between the gate terminal and the gate of the device.

6. A device as claimed in any one of claims 2 to 5 wherein the MOSFET has a vertical structure in that the gate and a source of the device are provided on one face of a chip body of the device and a drain of the MOSFET is provided on an opposite face of the body.

7. A device as claimed in claim 6 wherein the capacitor is integrated on the chip body.

8. A device as claimed in claim 7 wherein the capacitor is superimposed on the gate of the MOSFET.

9. A device as claimed in claimed in claim 5 wherein the capacitor is a discrete component connected in series between the gate and the gate terminal and packaged in the same package.

10. A device as claimed in any one of claims 5 to 9 wherein the gate is connected directly to a fourth terminal of the device.

11. A device as claimed in claim 9 wherein biasing resistors connected to the gate are included in the same package.